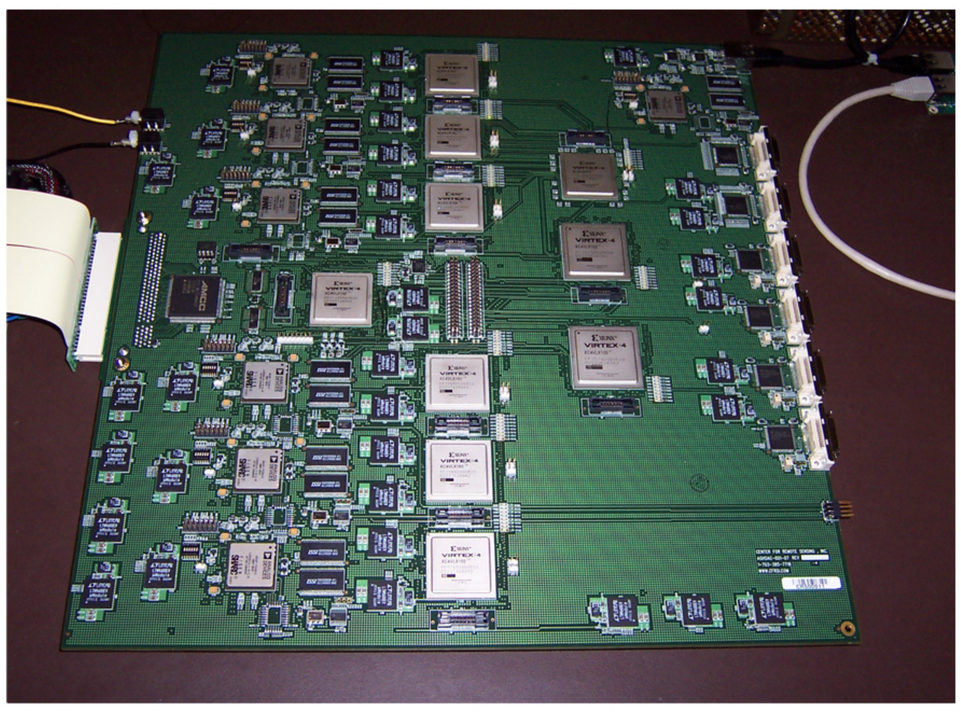
HIGH PERFORMANCE SIGNAL PROCESSING BOARD

(CRS--PROBRD--PCI-6DSP10FPGA-500M-08)



The CRS-PROBRD-PCI-6DSP10FPGA-500M-08 is a high performance processor board consisting of 10 high performance FPGAs and 6 DSPs specifically developed for large throughput high bandwidth RF sample generation and/or processing of high bandwidth samples. The board has a general purpose bus (PCI or PCI-X), a high bandwidth serial link for transferring data at more than 3 GBPS. Its main processors consist of 6 high performance Floating point DSPs at clock speed of 600 MHz and 8 top of the line Virtex IV/V FPGAs. The serial data links are connected directly to the FPGAs. Two combiner FPGAs are used to collect all the samples and connect to the high speed severed links. Thehigh speed links secured data transmission over significant distances. The board can also be used to process high bandwidth samples where the high speed bus is used for data input.

The high bandwidth data samples can be fed to DACs or coming from ADCs. The data samples can also be used to other boards for additional processing. Special care has been taken to ensure uniform clock propagation throughout the board.

There is an additional Virtex IV/V FPGA connected to the processor FPGAs for additional functions. Different versions of FPGAs in the Virtex IV or Virtex V series can be selected depending on the applications and nature of processing (i.e. number of multipliers, storage, logic, etc.). The card can be used for various applications and can provide a total processing capability of around 10 GFLOPS. The primary use for the card is the generation of high bandwidth RF signal samples used for various advanced real-time simulation.

The card has been used for generating up to 18 GPS satellite signals for all waveforms and all frequencies (L_1, L_2, L_5; C/A, P(Y), M, L_2C, L_5, etc.) with large update rate (up to 1 KHz). This provides a single card solution to complete navigation simulator. This allows precision generation of wavefronts necessary for phase array antenna simulation and other applications. The card can be used for generating variable delay lines with a large number of filter coefficients with fast update rates.

Various IP cores for all navigation (Galileo, Glonasss) and some communication and radar signals are currently available.

VARIOUS OTHER APPLICATIONS INVOLVE:

- Simulation of RF channels
- Delay line implementation for multiple channels with large number of taps
- Generation of complex waveforms
- Simulation of networked RF environments
- Simulation of radar
- Simulation of EW
- Simulation of Acoustic/Sonar

Schematics of the main core processors in the board is shown on the next page. The auxiliary processor and associated portions are omitted for clarity.

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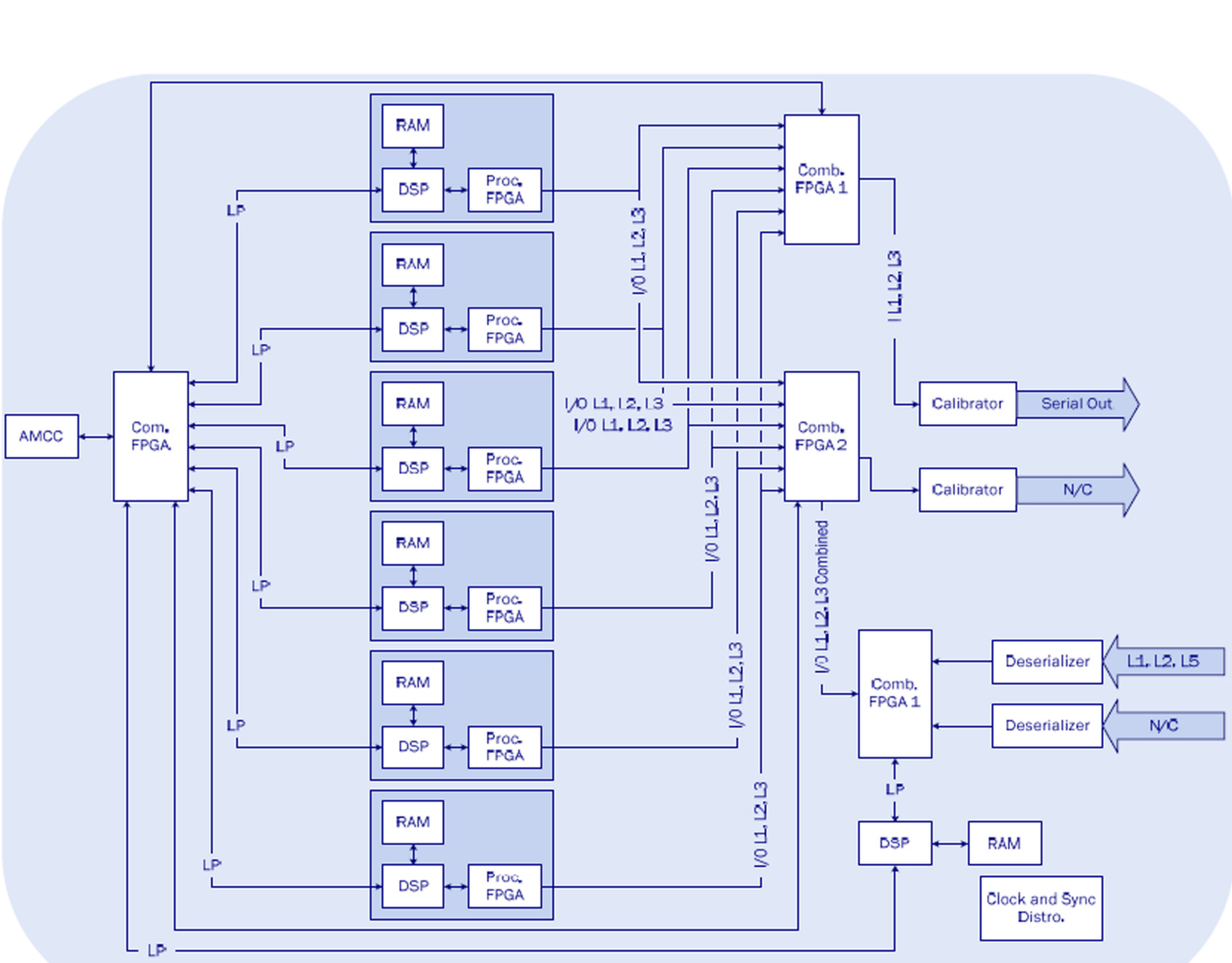
RF BOARD

SPECIFICATIONS

- General Purpose Bus: PCI/PCI Express
- Serial Bus: 4 SER/DES Interfaces, each with 800 MBPS
- Other Inferfaces: DIO, connector, Miktor, RJ45
- Main Processors: 6 Analog Devices Floating Point Processors (AD)
- Main Sample/Waveform Generators or Processors: 6 Xilinx Virtex IV/ Virtex V FPGAs (various processor options)
- Combination Processors: 2 Xilinx Virtex IV/ Virtex V FPGAs
- Auxilary Processor: 1 Xilinx Virtex IV/ Virtex V FPGAs
- Clock speeds: 600 MHz for DSPs, 250/400 MHz for FPGAs
- Total equivalent Processing capability: > 9 GFLOPS
- Size: 17” X 16.5” X 0.75”
- Power Consumption: Approx. 250 watts at full speed



Schematics of Antenna Card

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